METHOD AND APPARATUS FOR APPLICATION-SPECIFIC PROGRAMMABLE MEMORY ARCHITECTURE AND INTERCONNECTION NETWORK ON A CHIP

ABSTRACT

Programmable architecture for implementing a message processing system using an integrated circuit is described. In an example, specification data is received that includes attributes of the memory system. A logical description of the memory system is generated in response to the specification data. The logical description defines a memory component and a memory-interconnection component. A physical description of the memory system is generated in response to the logical description. The physical description includes memory circuitry associated with the integrated circuit defined by the memory component. The memory circuitry includes an interconnection topology defined by the memory interconnection component.